Design of a Field-Programmable Digital Filter Chip Using Multiple-Valued Current-Mode Logic

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SUMMARY This paper presents a Field-Programmable Digital Filter (FPDF) IC that employs carry-propagation-free redundant arithmetic algorithms for faster computation and multiple-valued current-mode circuit technology for high-density low-power implementation. The original contribution of this paper is to evaluate, through actual chip fabrication, the potential impact of multiple-valued current-mode circuit technology on the reduction of hardware complexity required for DSP-oriented programmable ICs. The prototype FPDF fabrication with 0.6 μm CMOS technology demonstrates that the chip area and power consumption can be reduced to 41% and 71%, respectively, compared with the standard binary logic implementation.

key words: multiple-valued logic, signal processor, FPGAs, FIR filters

1. Introduction

In many real-time Digital Signal Processing (DSP) applications, traditional microprocessor-based architectures are often inadequate to meet the requirements for intensive computation. Field-Programmable Gate Arrays (FPGAs) provide an alternative that maintains a rapid prototyping capability while providing performance levels significantly beyond that of programmable processors. If we introduce domain-specific FPGA architectures, further performance improvement is expected in specific DSP applications. Recently, several DSP-oriented FPGA architectures have been reported [1]–[3]. The key to success in designing specialized FPGA architectures for DSP relies on hardware algorithms that make possible not only higher performance but also lower circuit complexity. The problem of interconnection complexity has been recognized as a basic limitation in applying the reconfigurable computing technique for DSP tasks.

Addressing this problem, this paper presents a technique for implementing high-performance DSP-oriented FPGAs exhibiting both low power consumption and reduced circuit complexity. The proposed technique employs (i) binary SD (Signed-Digit) arithmetic [4]–[6] for high-speed multiply-add operations, and (ii) Multiple-Valued Current-Mode Logic (MV-CML) for significant reduction in wiring complexity. Figure 1 summarizes the impacts of the proposed technique for realizing a high-performance configurable signal processing architecture.

In this paper, we demonstrate the potential of the proposed technique in a typical application example—design of a specialized FPGA architecture for high-speed FIR filtering. The reference [7] has already proposed a high-speed programmable filter IC, called a Field-Programmable Digital Filter (FPDF)*, dedicated for signal processing and communication applications. The architecture was designed on the basis of ordinary binary logic circuits. In this paper, on the other hand, we propose a new design of FPDF based on the combination of MV-CML circuit technology and redundant arithmetic algorithms. The goal of this paper is to provide a case study to evaluate the impact of MV-CML on the reduction of hardware complexity required for DSP-oriented programmable ICs. A prototype chip of FPDF using MV-CML has been successfully designed and fabricated using 0.6 μm CMOS technology. The chip area and power consumption (@40 MHz operation) can be reduced to 41% and 71%, respectively, compared with the standard binary logic implementation described in [7].

*The FPDF architecture is dedicated to the implementation of FIR filters, and hence only the number of filter taps, the filter coefficients, datapath word length and mapping structure are programmable. To verify the potential of the proposed technique, further performance analysis is required assuming various different DSP tasks for practical applications.

Manuscript received November 22, 2002.
Final manuscript received April 14, 2003.
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2. Binary SD Arithmetic

This section describes binary Signed-Digit (SD) number representation, which allows high-speed arithmetic operations without carry propagation and is suitable for the implementation with Multiple-Valued Current-Mode Logic (MV-CML). The SD number representation is a redundant representation using a symmetrical digit set \{-1, 0, 1\}. Any integer \(X\) can be represented as a sequence of radix-2 signed digits \(X_i\) as follows:

\[
X = [X_{n-1}X_{n-2}\cdots X_1X_0]_{SD2}
\]

(1)

where \(X_i\) \(\in\{-1, 0, 1\}\).

Consider two binary SD numbers:

\[
X = [X_{n-1}\cdots X_i\cdots X_0]_{SD2},
\]

(2)

\[
Y = [Y_{n-1}\cdots Y_i\cdots Y_0]_{SD2}.
\]

(3)

The addition of these two numbers is performed by the following three steps in each digit:

**Step 1:** \(Z_i = X_i + Y_i\),

**Step 2:** \(2C_i + W_i = Z_i\),

**Step 3:** \(S_i = W_i + C_{i-1}\),

where \(Z_i, W_i, C_i\) and \(S_i\) are the linear sum, the intermediate sum, the carry and the final sum, respectively. Each variable takes the following range:

\(X_i, Y_i, S_i, C_i \in \{-1, 0, 1\}\),

\(Z_i \in \{-2, -1, 0, 1, 2\}\),

\(W_i \in \{-1, 0\}\) (if \(Z_{i-1} > 0\)),

\(W_i \in \{0, 1\}\) (if \(Z_{i-1} \leq 0\)).

Step 2 decomposes the linear sum \(Z_i\) into the intermediate sum \(W_i\) and the carry \(C_i\) so that the dynamic range of the final sum \(S_i\) created in Step 3 may fit within the range from -1 to 1. Table 1 and Fig. 2 show how to generate \(W_i\) and \(C_i\) from \(Z_i\) in Step 2. Since the carry \(C_i\) can be computed without referring the lower-digit carry \(C_{i-1}\), carry-propagation-free addition can be achieved. Figure 3 shows an example of binary SD addition.

3. Binary SD Adder Using MV-CML

This section describes the implementation of the binary SD adder using Multiple-Valued Current-Mode Logic (MV-CML) technology [5], [8]. In MV-CML, each digit \(\{-1, 0, 1\}\) for binary SD arithmetic can be represented by bidirectional current on a wire; the sign (+ or -) is represented by current direction (positive or negative) and the digit magnitude is represented by current level (amount).

Figure 5 shows the basic building blocks for MV-CML used in our design. Threshold detectors, which compare the amount of input current and that of reference current, are the most characteristic components in MV-CML circuits. In the following, we explain the operation of the pMOS Type-B threshold detector (Type-B pTD) in detail as an example (see the portion marked...
Fig. 5 Basic MV-CML circuits, where $I_0$ is the unit current ($I_0 = 10 \mu A$ in our design).

One of the most important features of MV-CML is that linear summation can be performed by wiring without any active devices. This makes possible drastic reduction in the number of transistors in arithmetic circuits. Figure 6 shows the MV-CML implementation of the binary SD full adder (SDFA) described in the last section. The linear summation operations for Step 1 and Step 3 are implemented by simple wiring points. The most of the circuit resources are devoted for Step 2, which accepts the bidirectional current sum $Z_i$ and generates $W_i$ and $C_i$. The bidirectional current $Z_i$ is copied to unidirectional currents $I_1 \sim I_2$ or to $I_3 \sim I_5$ depending on the current direction. The threshold detectors produce the binary voltage signals $V_1 \sim V_5$, which control the switching of 10 pass transistors. These pass transistors form a pair of series-parallel logic circuits to implement the transfer characteristics for $W_i$ and $C_i$ as illustrated in Fig. 2. For example, $W_i = -1$ (i.e., $-I_0$) when $(V_2 \text{ OR } V_3) \text{ AND } \overline{V_6} = \text{HIGH}$.

Figure 7 shows the transfer characteristics for the binary SDFA obtained by HSPICE simulation, where standard 0.6 $\mu$m CMOS technology is employed. The unit current $I_0$ corresponding to the digit value 1 is 10 $\mu$A. The unit current determines the maximum operating frequency of MV-CML circuits. We derive the condition $I_0 = 10 \mu A$ from our target frequency 50 MHz. The unit current 10 $\mu$A is about 1/20 of short-circuit current in a CMOS inverter.

The current sources are most important components in MV-CML circuits since they are used to produce the output signals of functional modules as well as the reference signals for threshold detectors. In our
design, the unit current $I_0$ is programmed as 10 $\mu$A by controlling the transistor sizes ($W$ and $L$) of current sources, and their gate bias voltages $V_p$ and $V_n$. We use transistors with the channel length $L = 1.5 \times L_{\text{min}} \sim 2 \times L_{\text{min}}$ as current sources, where $L_{\text{min}}$ denotes the minimum channel length of a transistor. Thus, we can use fairly small transistors in MV-CML circuits compared with ordinary analog circuits. The operation of MV-CML circuits is not so sensitive to $V_t$ variation, since a designer must guarantee the correct circuit operation only for a limited range of discrete operating points: $-20 \mu$A, $-10 \mu$A, 0 $\mu$A, 10 $\mu$A and 20 $\mu$A.

Note that MV-CML can carry a single digit ($\in \{-1, 0, 1\}$) of binary SD representation on a single wire. On the other hand, ordinary binary logic implementation requires a pair of wires to convey a single digit of SD representation since the digit set $\{-1, 0, 1\}$ must be encoded into binary vectors, such as $[10, 00, 01]$. Thus, 50% reduction in the number of I/O interconnections is expected for the MV-CML SDFA compared with the binary logic implementation.

Also, the current summation technique of MV-CML, which does not require any active devices, makes possible further reduction in the number of interconnections. For example, assume that we would like to send a pair of SD operands $X_i$ and $Y_i$ ($\in \{-1, 0, 1\}$) that should eventually be added at a specific destination. In voltage-mode binary logic implementation, we need 4 wires to transmit the SD operands $X_i$ and $Y_i$ independently. In MV-CML circuits, on the other hand, the two SD operands are represented by a pair of birectional current signals. Assuming the two numbers will be summed up at the receiver end, it may be a good idea to pack $X_i$ and $Y_i$ by current summation before transmission; thus, we transmit a 5-level current signal ($\in \{-2, -1, 0, 1, 2\}$) on a single interconnection. (Note that we need an SDFA to reduce the signal range from $\{-2, -1, 0, 1, 2\}$ to $\{-1, 0, 1\}$ at the receiver end.) This technique can reduce the number of interconnects in MV-CML circuits to 25% ($=1/4$) compared with the binary logic implementation. This property is particularly useful for DSP-oriented FPGA devices, in which efficient implementation of arithmetic operations is required.

4. Designing FPDF Using MV-CML

4.1 Architecture

This section describes the design and implementation of a Field-Programmable Digital Filter (FPDF)—a programmable filter IC for high-speed FIR filtering dedicated for signal processing and communication applications [9], [10]. We choose FIR filter application in order to demonstrate the potential of the proposed technique—the combination of redundant arithmetic algorithms and MV-CML circuit technology—for high-speed, low-power and compact implementation of DSP-oriented programmable ICs. This technique will also be effective in other applications, in which efficient implementation of multiply-add operation is required.

Figure 8 illustrates the overall architecture of the FPDF, which consists of Configurable Arithmetic Blocks (CABs), Connection Blocks (CBs), Switch Blocks (SBs) and Product Generators (PGs). The basic structure of FPDF is similar to those of conventional FPGAs—building blocks are connected by programmable interconnects. Major difference is that FPDF employs an 8-bit latched SD adder as a functional block (called the CAB) instead of Configurable Logic Blocks (CLBs) used in typical FPGAs. These CABs are connected by programmable current-mode interconnections according to configuration data downloaded into FPDF in advance. Each current-mode interconnection can convey a 3-valued signal $\{-1, 0, 1\}$ or a 5-valued signal $\{-2, -1, 0, 1, 2\}$ as described in the last section. The routing elements, CBs and SBs, are used to guide the bidirectional current signals from source CABs to destination CABs.

Figure 9 illustrates how to map an FIR filter structure onto basic components of FPDF, where the word length of the filter is 8 bits in this example. The filter coefficients are encoded by Canonical Signed-Digit (CSD) representation [11]. The multiplications between the input signal and CSD coefficients are performed by PGs followed by CABs. The pipelined accumulation of generated products is performed by CABs to produce the output of the FIR filter. For pipeline,
a CAB contains an 8-bit register, which could be bypassed when it is used for CSD multiplication. Bidirectional current summation is fully utilized for pipelined accumulation leading to drastic reduction in interconnection complexity.

### 4.2 Functional Blocks for FPDF

This subsection describes the design of basic functional blocks for FPDF, where every functional block is newly designed using MV-CML circuit technology. The use of MV-CML makes possible significant reduction in the number of programmable interconnects, which leads to compact implementation of CBs and SBs. Also, direct implementation of SD arithmetic using MV-CML without binary encoding allows high-speed low-power implementation of CBs. In the following, we describe the newly designed MV-CML functional blocks in detail.

CAB (Configurable Arithmetic Block) is an 8-bit latched binary SD adder with no carry propagation chain. Figure 10(a) shows the 1-bit circuit for CAB. MV-CML circuit technology is used to implement the CAB circuit except for latches for pipelining; the latches employ conventional voltage-mode circuits and could be bypassed by selectors when combinational operation is required. Figure 10(b) shows the layout of CAB using 0.6-μm CMOS triple-metal technology. Note that this circuit implements Step 2 and Step 3 of binary SD addition, while Step 1 is realized by simple current summation on an input wire.

There are two routing elements in FPDF, that is, CB (Connection Block) and SB (Switch Block). Figure 11 shows the structure of CB, which consists of nMOS switches for wire routing and SRAM cells for controlling the nMOS switches. CBs are used not only for programmable routing, but also for current summation by wiring (Step 1 of binary SD addition); if two current signals are connected to a common interconnection, these signals are added together to form a 5-level current signal (∈ {−2, −1, 0, 1, 2}), resulting in 25% reduction in the number of interconnects. On the other hand, SB shown in Fig. 12 is a switch matrix placed at an intersection of vertical and horizontal data lines.

PG (Product Generator) shown in Fig. 13, which
is placed at the first stage of FPDF architecture, generates a product between an 8-bit input signal and an 8-digit CSD coefficient (that contains four nonzero digits (−1 or 1) at most). The sign-vector conversion technique of Signed-Weight (SW) arithmetic [7] is used to control the sign of partial products so that we can pack every four partial products into a single 8-digit string of 5-valued digit \((-2, -1, 0, 1, 2)\).

This product generation algorithm is explained in Fig. 14. Let assume that the coefficient of multiplication is \(0.1011011_2 (= 0.7109375)\) in two’s complement binary number system. This coefficient can be converted into CSD coefficient as \(1.0101010_{CSD2}\), which contains four nonzero digits. Assume also that the input to the FIR filter is \(0.1011010_2\) in two’s complement binary number system. Multiplication between the input and the CSD coefficient produces the four partial products (corresponding to the four nonzero digits in the CSD coefficient). Note that the first partial product has positive sign and the other three partial products have negative signs as shown in Fig. 14. For making efficient use of sign-symmetric number representation in SD notation, we need to balance the number of positive and negative partial products. Thus, in Fig. 14, the sign of the 4th partial product is flipped into positive by introducing negative bias quantity as a side effect (the bias thus introduced should be canceled at the final-stage adder in the FPDF architecture). As a result, we have two positive partial products and two negative partial products. By adding every pair of positive and negative partial products, we can convert the four partial products into two partial products in binary SD number representation. Note that these two binary SD products must be added at CAB in the succeeding stage as shown in Fig. 9. For this purpose, PG generates a single 5-valued signal by packing two binary SD products with current summation in advance. The CAB at the next stage receives this packed signal and converts it into binary SD notation. Figure 15 illustrates another example of product generation for the CSD coefficient \(0.0101011_{CSD2} (= 0.3359375)\). As
shown in this example, the sign vector conversion technique makes possible to generate a pair of SD partial products for arbitrary CSD coefficients. The side effect of this process—the bias quantity—must be canceled at the final stage adder. This bias cancelling process is illustrated in Fig. 16.

The above example illustrates 8-bit CSD coefficient multiplication. The wordlength of internal datapath can be extended to any multiple of 8 bits by cascading the carry-out/carry-in signals of CABs. Input/output data length, on the other hand, cannot be extended in our present design due to the limited number of I/O pins.

4.3 Performance Evaluation

This section compares the proposed MV-CML FPDF with the corresponding voltage-mode binary logic implementation (using SW arithmetic) [7]. The binary logic FPDF considered here is based on the design described in [7], where each CAB employ a 4-2 counter with no carry propagation chain. Also, the binary logic FPDF does not employs PGs, since the partial product generation is performed by CBs through simple shift operations. Both FPDFs (binary logic and MV-CML) are dedicated to high-speed FIR filter realization and have the same function. The major design parameters, such as wordlength and data line width, are almost same for both designs.

For comparison, we designed both FPDFs using the same 0.6 µm CMOS triple-metal technology. Figure 17 compares the layout of MV-CML FPDF with that of binary-logic FPDF on a 4.4 mm × 4.4 mm chip. Binary-logic FPDF integrates 22 CABs on a chip and can implement an 11-tap FIR filter at most. On the other hand, MV-CML FPDF integrates 60 CABs on a chip and can implement a 30-tap FIR filter at most. When mapping an 11-tap FIR filter, binary-logic FPDF
Table 2  Comparison of FPDF chip features.

<table>
<thead>
<tr>
<th></th>
<th>Binary-Logic FPDF</th>
<th>MV-CML FPDF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input data/Output data</td>
<td>8 bit/16 bit (two'complement)</td>
<td>8 bit/8 bit (two'complement)</td>
</tr>
<tr>
<td>Maximum filter tap</td>
<td>11-tap</td>
<td>30-tap</td>
</tr>
<tr>
<td>Transistor count</td>
<td>109,704 Transistors</td>
<td>150,247 Transistors</td>
</tr>
<tr>
<td>Chip size</td>
<td>4.4 mm × 4.4 mm</td>
<td></td>
</tr>
<tr>
<td>Effective size</td>
<td>3.0 mm × 3.0 mm</td>
<td>3.4 mm × 3.5 mm</td>
</tr>
<tr>
<td>Process</td>
<td>0.6 µm CMOS triple metal layers</td>
<td></td>
</tr>
<tr>
<td>Active area size</td>
<td>9.0 mm² [109,704 Transistors]</td>
<td>3.7 mm² [51,891 Transistors]</td>
</tr>
<tr>
<td>for an 11-tap FIR filter</td>
<td>10 MHz 24 mW</td>
<td>3.0 mm × 3.0 mm</td>
</tr>
<tr>
<td>Power consumption</td>
<td>20 MHz 48 mW</td>
<td>4.7 mm × 4.5 mm</td>
</tr>
<tr>
<td>for an 11-tap FIR filter</td>
<td>30 MHz 73 mW</td>
<td>5.6 mm × 5.7 mm</td>
</tr>
<tr>
<td>(HSPICE simulation)</td>
<td>40 MHz 96 mW</td>
<td>6.8 mm × 6.9 mm</td>
</tr>
</tbody>
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Fig. 18  Layouts of basic building blocks.

requires active area of 9.0 mm², while MV-CML FPDF requires only 3.7 mm². Thus, the use of MV-CML technology makes possible to reduce the active area to 41% in comparison with binary logic implementation. The transistor count and power consumption (@40 MHz operation) are also reduced to 47% and 71%, respectively.

Table 2 summarizes the result of comparison. The output data length of MV-CML FPDF is 8 bits simply because the wordlength of the final stage adder on a fabricated chip is 8 bits. We can easily extend the wordlength of the final stage adder to 16 bits with only 1% increase in transistor count. Note that there are no essential differences in the functionality between binary logic FPDF and MV-CML FPDF. The wordlength of internal datapath for both designs can be extended to any multiple of 8 bits by changing configuration data.

Figure 18 compares the layouts of basic building blocks for binary-logic FPDF with those for MV-CML FPDF. The size of CAB is almost same for both designs. As for routing elements, such as CBs and SBs, MV-CML FPDF requires much less area on a chip due to the reduction in the number of programmable interconnections by using multi-level current-mode signaling. Figure 19 shows the enlarged view of the layout of MV-CML FPDF.

A major disadvantage of MV-CML circuit technology is its limited range of operating frequency. In our design, the unit current (current for digit value 1) is 10 µA. In this case, the maximum operating frequency is limited to 40 MHz, while the binary-logic implementation reaches 90 MHz. In order to achieve higher performance, we need to increase the unit current of MV-CML circuits. For example, if we introduce higher unit current, say 30 µA, we can achieve 85 MHz operation†.

In this case, however, relatively higher power dissipation in low-frequency region may be a major problem. In order to resolve the tradeoff between speed and

†HSPICE simulation shows that we can change the unit current within the range 10–40 µA simply by changing the bias voltages \( V_p \) and \( V_n \) for current sources. We must change the transistor sizes (\( W \) and \( L \)) in order to change the unit current beyond this range.
power, application specific consideration is required for selecting optimal value of unit current. Variable-unit-current approach should also be explored for future applications.

We have designed and fabricated an MV-CML FPDF chip shown in Fig. 17(b). The valid operation is successfully confirmed by mapping various FIR filters having a tap count up to 30. Figure 20 shows an example of chip measurement using an LSI tester (Advantest T6671E). The critical delay is measured by connecting the basic components: PG, SB, CB, CAB, CB, and the final stage adder, in series (bypassing all the latches in CAB). In this particular case, the measured critical delay is 90 ns, which significantly depends on the circuit configuration mapped onto the FPDF.

5. Conclusion

In this paper, we proposed a technique for implementing high-performance DSP-oriented FPGAs exhibiting low power consumption and reduced circuit complexity. The technique employs (i) binary SD (Signed-Digit) arithmetic for high-speed multiply-add operations, and (ii) multiple-valued current-mode logic (MV-CML) for reducing wiring complexity. We need to verify the potential of the proposed technique in various different DSP tasks for practical application.

Acknowledgments

The VLSI chip in this study has been fabricated under the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

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